1. A method of forming a second metal structure, overlying and contacting an underlying first metal structure, comprising the steps of:

forming an opening in an interlevel dielectric (ILD) layer;

forming said first metal structure in said opening in said ILD layer;

depositing a first metal layer, to be used as an adhesive metal layer;

depositing a second metal layer;

depositing an insulator layer;

forming a photoresist shape on said insulator layer, with said photoresist shape overlying a portion of underlying, said first metal structure;

performing a first dry etch procedure to remove a region of said insulator layer, and to remove a top portion of said second metal, not covered by said photoresist shape, creating a partially etched metal structure comprised with an overlying portion of unetched insulator layer;

removing said photoresist shape;

forming insulator spacers on sides of partially etched metal structure, resulting in a wider partially etched metal structure; and

using said wider partially etched metal structure as an etch mask, performing a second dry etch procedure removing an exposed bottom portion of said second metal layer, and removing an exposed portion of said first metal layer, resulting in definition of said second metal structure, with said second metal structure completely covering underlying, said first metal structure.

2. The method of claim 1, wherein said interlevel dielectric (ILD) layer is a silicon oxide, or boro-phosphosilicate glass (BPSG) layer, obtained via LPCVD or PECVD procedures at a thickness between about 4,000 to 10,000 Angstroms.

3. The method of claim 1, wherein said opening, in said ILD layer, is comprised with a diameter between about 0.2 to 1.2 um.

4. The method of claim 1, wherein said first metal structure is a metal plug structure, comprised of a metal chosen from a group containing aluminum, aluminum - copper, copper, or tungsten.

5. The method of claim 1, wherein said first metal layer, used as said adhesive metal layer, is a titanium layer, obtained via plasma vapor deposition (PVD) procedures at a thickness between about 500 to 2,000 Angstroms.

6. The method of claim 1, wherein said second metal layer is chosen from a group containing aluminum, aluminum - copper, copper, or tungsten, obtained via PVD procedures at a thickness between about 5,500 to 6,500 Angstroms.

7. The method of claim 1, wherein said insulator layer is a silicon oxide layer obtained via PECVD procedures at a thickness between about 1,500 to 2,500 Angstroms, using tetraethylorthosilicate (TEOS) as a source.

8. The method of claim 1, wherein said photoresist shape is comprised with a width between about 0.2 to 1.2 um.

9. The method of claim 1, wherein said first dry etch procedure, used to form said partially etched metal structure, is performed using an anisotropic RIE procedure, employing CHF_3 as an etchant for said insulator layer, and using Cl_2 or SF_6 as an etchant for said top portion of said second metal layer.

10. The method of claim 1, wherein the thickness of said top portion of said second metal layer removed during said first dry etch procedure is between about 2,000 to 3,000 Angstroms.

11. The method of claim 1, wherein said insulator spacers are silicon oxide spacers, formed at a thickness between about 350 to 450 Angstroms, via deposition of a silicon oxide layer, using LPCVD or PECVD procedures, than defined via a selective, anisotropic RIE procedure, using CHF_3 as an etchant for silicon oxide.

12. The method of claim 1, wherein said wider partially etched metal structure is between about 700 to 900 Angstroms wider than the width of said partially etched metal structure.

13. The method of claim 1, wherein said second dry etch procedure used to define said second metal structure, is an anisotropic RIE procedure using Cl_2 or SF_6 as an etchant for said bottom portion of said second metal layer and for said first metal layer.

14. A method of forming a metal line structure featuring insulator spacers formed on a top portion of a partially defined metal line structure, used to reduce the risk of exposing an underlying metal plug structure to final stages of a dry etch procedure used to define said metal line structure, comprising the steps of:

providing a conductive region;

forming an ILD layer on said conductive region;

forming an opening in said ILD layer exposing a portion of top surface of said conductive region;

depositing a first metal layer;

removing a portion of said first metal layer from top surface of said ILD layer resulting in formation of said metal plug structure in said opening;

depositing a titanium layer;

depositing a second metal layer;

depositing a silicon oxide layer;

forming a photoresist shape on said silicon oxide layer, with said photoresist shape overlying a portion of, or all of underlying, said metal plug structure;

performing a first anisotropic reactive ion etch (RIE) procedure to remove the region of said silicon oxide layer and to remove of a top portion of a region of said second metal, not covered by said photoresist shape, creating a partially etched metal line structure, comprised with an overlying, etched silicon oxide shape;

depositing an insulator layer;

performing a second anisotropic RIE procedure to form said insulator spacers on sides of said partially etched metal line structure, resulting in a wider partially etched metal line structure; and

performing a third anisotropic RIE procedure, using said wider partially etched metal line structure as an etch mask, to remove an uncovered bottom portion of said second metal layer, and to remove an uncovered portion of said titanium layer, resulting in definition of said second metal line structure, with said second metal line structure completely covering underlying, said metal plug structure.

15. The method of claim 14, wherein said conductive region is an underlying metal structure, or an active device region in a semiconductor substrate, such as a heavily doped source/drain region.

16. The method of claim 14, wherein said ILD layer is a silicon oxide, or boro-phosphosilicate glass (BPSG) layer, obtained via LPCVD or PECVD procedures at a thickness between about 4,000 to 10,000 Angstroms.

17. The method of claim 14, wherein said opening, in said ILD layer, is comprised with a diameter between about 0.2 to 1.2 um.

18. The method of claim 14, wherein said metal plug structure, located in said opening in said ILD layer, is comprised with a metal chosen from a group containing aluminum, aluminum - copper, copper, or tungsten.

19. The method of claim 14, wherein said titanium layer is obtained via plasma vapor deposition (PVD) procedures at a thickness between about 500 to 2,000 Angstroms.

20. The method of claim 14, wherein said second metal layer is chosen from a group containing aluminum, aluminum - copper, copper, or tungsten, obtained via PVD procedures at a thickness between about 5,500 to 6,500 Angstroms.

21. The method of claim 14, wherein said silicon oxide layer is obtained via PECVD procedures at a thickness between about 1,500 to 2,500 Angstroms, using tetraethylorthosilicate (TEOS) as a source.

22. The method of claim 14, wherein said photoresist shape is comprised with a width between about 0.2 to 1.2 um.

23. The method of claim 14, wherein said first anisotropic RIE procedure, used to form said partially etched metal line structure, is performed using CHF_3 as an etchant for said silicon oxide layer, and using Cl_2 or SF_6 as an etchant for said top portion of said second metal layer.

24. The method of claim 14, wherein the thickness of said top portion of said second metal layer removed during said first anisotropic RIE procedure is between about 2,000 to 3,000 Angstroms.

25. The method of claim 14, wherein said insulator layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between about 350 to 450 Angstroms, using TEOS as a source.

26. The method of claim 14, wherein said insulator spacers are defined using said second anisotropic RIE procedure, employing CHF_3 as an etchant for silicon oxide.

27. The method of claim 14, wherein said third anisotropic RIE procedure, used to define said metal line structure, is performed using Cl_2 or SF_6 as an etchant for said bottom portion of said second metal layer and for said titanium layer.